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Notice of Allowability	**Application No.** 10/677,438	**Applicant(s)** ESTEPA ET AL.	
	Examiner Michael K. Luhrs	**Art Unit** 2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 3/3/2005.
2. ☒ The allowed claim(s) is/are 1,3-7,9-14 and 21-25.
3. ☒ The drawings filed on 02 October 2003 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other updated search.

DETAILED ACTION

1. Examiner acknowledges claim of priority to Provisional Application Serial No. 60/483,457 as indicated in applicant's amdt dtd. 1/16/2004.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this examiner's amendment was given in a telephone interview with Attorney Tung on 5/16/05.

4. In claim 1, line 12, replace "whereby" with –thereby—

5. In claim 21, line 9, replace "whereby" with –thereby—

The application has been amended as follows:

1. A method of assembling an integrated circuit (IC) device
with a substrate, comprising:
providing a substrate having electrical terminals on a first side of the substrate, and
a copper bondpad on a second side of the substrate opposing the first side
electrically coupled to at least one of the terminals;
the copper bondpad being substantially free of plated gold and substantially free of
solder material;
mounting the IC chip to the first side of the substrate;
electrically connecting the IC chip to the terminals;
encapsulating the IC chip mounted on the substrate with encapsulation material at
an elevated temperature, ~~whereby~~ thereby oxidizing the surface of the copper bondpad;

spraying an aqueous etchant on the bondpad to remove oxidized copper
from the bondpad; and
coating the etched bondpad with an anti-tarnish solution.

21. A method of forming an integrated circuit (IC) device with an improved
substrate, comprising:
providing a substrate having terminals on a first side and copper bondpads on
a second side, the outer surface of the copper bondpads substantially free of plated gold,
substantially free of plated nickel, and substantially free of solder material;
attaching an integrated circuit chip on the first side and electrically connecting the
chip to the terminals;
encapsulating the circuit chip attached to the substrate with encapsulation material
at an elevated temperature ~~whereby~~ thereby oxidizing the surface of the copper bondpads;
submerging the substrate with the encapsulated IC chip in an aqueous etchant to
remove oxidized copper from the bondpads; and
coating the etched bondpads with an anti-tarnish solution.

Allowable Subject Matter

6. Claims 1, 3-7, 9-14 and 21-25 are allowed.

7. The following is an examiner's statement of reasons for allowance: Regarding claim 1, there was no teaching or suggestion in the prior art of the *providing a substrate having electrical terminals on a front side of the substrate and a copper bondpad on a second side of the substrate opposing the first side electrically coupled to at least one of the terminals; the copper bondpad being substantially free of plated gold and substantially free of solder material, mounting the IC chip to the first side of the substrate, electrically connecting the IC chip to the terminals; encapsulating the IC chip mounted on the substrate with encapsulation material at an elevated temperature thereby oxidizinq the surface of the copper bondpad; spraying an aqueous etchant on the bondpad to* *remove oxidized copper, and coating the etched bondpad with an anti-tarnish solution.* Claims 3-7 and 7-14 dependent thereto are thereby also allowed.

Regarding claim 21, there was no teaching or suggestion in the prior art of the *providing a substrate having terminals on a first side and copper bondpads on a second side, the outer surface of the copper bondpads substantially free of plated gold, substantially free of plated nickel, and substantially free of solder material; attaching an integrated circuit chip on the first side and electrically connecting the [integrated circuit] chip to the terminals; encapsulating the [integrated] circuit chip attached to the substrate with encapsulation material at an elevated temperature thereby oxidizing the surface of the copper bondpads; submerging the substrate with the encapsulated IC [integrated circuit] chip in an aqueous etchant to remove oxidized copper from the bondpads; and coating the etched bondpads with an anti-tarnish solution.* Claims 22-25 dependent thereto are thereby also allowed.

It was found that the prior art typically coats the PCB with anti-tarnish and while encapsulant on the chip typically prevents oxidizing, however the prior art does not mention oxidization of the copper bondpad, located on the second side of the substrate, as a result from the encapsulation at elevated temperature, with the IC chip [already] electrically coupled to at least one of terminals on the first side of the substrate.

Closest art is: Li et. al. USPN 6,358,847 who teach the removal of the oxide from the bondpad. This bondpad is for the wire bonding area, and there is no mention of bondpad on second side, albeit does mention other packaging technologies (line 44-5, col. 3), yet there is no mention of the relationship to the oxide resulting from encapsulation. And Lindgren, USPN 6,593,221 submerges in SiO_2 solution for backside passivation, yet this does not substantially plate out onto the bondpads (lines 24-5, col. 6). Haji USPN 5,909,633 teach a plasma clean of the [gold] bondpad on second substrate surface after encapsulation.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. McCormick USPN 6,431,432 clearly teach that the OSP is applied to the substrate bond pads in lines 62-3, col. 3. Allardyce et. al. USPN 5,106,454 teach the sulphuric acid to rid the copper oxide from printed circuit boards. Kirsten USPN 6,367,150 teaches a solder flux that, when heated, cleans metal oxides from metal surfaces on the chip, see also PGPUB 2002/0095783 by Kirsten. Leuenberger et. al. USPN 6,420,207 teach the <u>OSP on to the ball side</u> yet there is no mention of relationship to the encapsulant, albeit, both OSP and gold plating for the wire bond are discussed in column 6. USPN PGPUB 2003/0216025 teach a wafer dip copper plating, and the anti-tarnish [0066] [0067].

Eichelberger et. al. USPN 6,396,148 teach the processing for all gold, copper, and nickel bond pads, col. 9. Sambucetti et. al. USPN 6,335,104 teaches the preparation acid clean of the copper pad follows with noble metal.

By the assignee: Yunus et. al. PGPUB 2004/0150105, and USPN 6,696,757, teach the OSP constituents and OSP directly on the copper pads. [0032] and line 19+, col. 5 respectively.
Scanlon, et. al. USPN 6,494,361 teaches the OSP on both sides, see the discussion column 4.

Wang et. al. USPGPUB 2004/0087057 teaches the pillars, the terminals and the pads are all copper. Sajja et. al. USPN 5,313,021 teach that the OSP on the PCB copper pads is well known, col. 7,line 10+. See also Sajja et. al. USPN 5,400, 948.
Maeda et. al. USPN 6,7`13,318 teach no-clean flux for C4. Hymes USPN 6,423,200 teach removal of oxide from copper seed layer.
Lu et. al. PGPUB 2003/0216025 teach anti-tarnish onto copper bump.
Test et. al. USPN 6,800,555 teach a barrier metal coating to copper.
Grieser et. al. USPN 6,562,149 copper pre-treatment.
Condra et. al. USPN 5,304,252 teach putting the anti-tarnish directly in the solder mask stripper solution.
Sawa et. al. USPN 3,933,531 teach copper anti-tarnish.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael K. Luhrs whose telephone number is 571-272-1874. The examiner can normally be reached on M-F, 8-5.

11. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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05/06/2005

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